CLAIMS

1. (Currently amended) A solid-state image sensor having a readout architecture that incorporates charge multipliers, said image sensor including:

a first CCD register adjacent to at least a second CCD register and coupled to the said first register through a charge overflow barrier, where charge may overflow during transfer, and where the width of the CCD registers varies in proportion to the increasing amount of charge depending on the number of CCD stages that include charge multiplication devices.

2. (Previously Amended) The image sensor according to claim 1 wherein the second adjacent CCD register collects overflow charge and transports it to at least one detection node located in each register, and each charge detection node having charge conversion sensitivity that may be different for each node.

3. (Original) The image sensor according to claim 2, wherein signals from adjacent register detection nodes are processed and combined according to a predetermined mathematical formula.

4. (Presently Amended) A solid-state image sensor having a readout architecture that incorporates charge multipliers, said image sensor including:

a CCD register that incorporates at least one charge-multiplication device element in at least one stage and said at least one stage has a progressively wider width;

wherein the width of the CCD register-stages and the number of charge-multiplication elements in at least some of its stages varies according to a predetermined formula.

5.(Cancelled)

6. (Presently amended) The image sensor according to claim ~~5~~ 4, wherein the predetermined formula has an exponential dependency on the number of CCD stages that include charge multiplication devices.

7. Cancelled

8. (Currently Amended) The image sensor according to claim 4, wherein the CCD register has a charge overflow barrier and a charge overflow drain incorporated in at least one of its stages to prevent charge blooming in the direction of charge transfer.

9. (Currently Amended) A solid-state image sensor having a readout architecture, said readout architecture incorporating:

charge multipliers;

CCD registers; and

a charge overflow device in at least one of its registers; wherein the width of the CCD register-stages and the number of charge-multiplication elements in at least some of its stages varies according to a predetermined formula which has an exponential dependency on the number of CCD stages that include charge multiplication devices.

10 Cancelled